

Precision Analog Controller

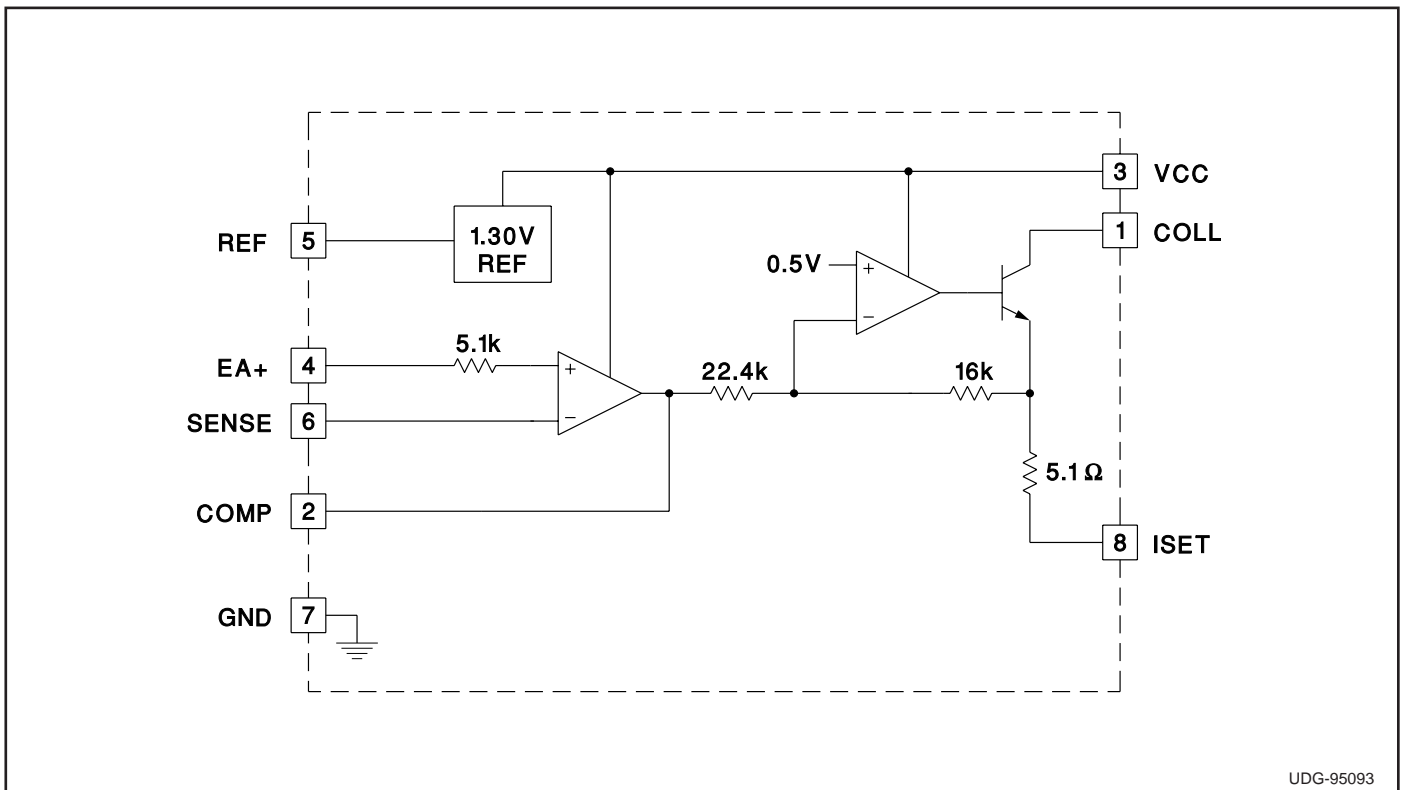
FEATURES

- Programmable Transconductance for Optimum Current Drive
- Accessible 1.3V Precision Reference
- Both Error Amplifier Inputs Available
- 0.7% Overall Reference Tolerance
- 0.4% Initial Accuracy
- 2.2V to 36.0V Operating Supply Voltage and User Programmable Reference
- Reference Accuracy Maintained for Entire Range of Supply Voltage
- Superior Accuracy and Easier Compensation for Optoisolator Application
- Low Quiescent Current (0.50mA Typ)

DESCRIPTION

The UC39432 is an adjustable precision analog controller with 100mA sink capability if the ISET pin is grounded. A resistor between ISET and ground will modify the transconductance while decreasing the maximum current sink. This will add further control in the optocoupler configuration. The trimmed precision reference along with the non-inverting error amplifier inputs are accessible for custom configuration. A sister device, the UC39431 adjustable shunt regulator, has an on-board resistor network providing six preprogrammed voltage levels, as well as external programming capability.

BLOCK DIAGRAM



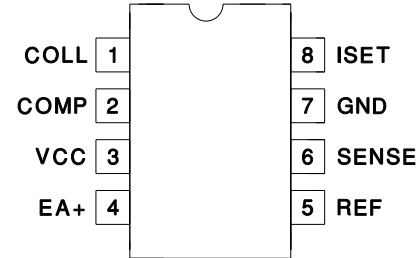
ABSOLUTE MAXIMUM RATINGS

Supply Voltage: VCC	.36V
Regulated Output: V _{COLL}	.36V
EA Input: SENSE, EA+	.6V
EA Compensation: COMP	.6V
Reference Output: REF	.6V
Output Sink Current: I _{COLL}	.140mA
Output Source Current: ISET	–140mA
Power Dissipation at T _A ≤ 25°C (DIL-8)	.1W
Derate 8mW/°C for T _A > 25°C	
Storage Temperature Range	–65°C to +150°C
Junction Temperature	–55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Currents are positive into, negative out of the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-8, SOIC-8 (Top View)
N or J, D Package



ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C and COLL Output = 2.4V to 36.0V for the UC19432, T_A = –25°C to +85°C and COLL Output = 2.3V to 36.0V for the UC29432, and T_A = 0°C to +70°C and COLL Output = 2.3V to 36.0V for the UC39432, VCC = 15V, I_{COLL} = 10mA, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Reference Voltage Tolerance	T _A = 25°C	19432*	1.295	1.3	1.305	V
		39432B	1.29	1.3	1.31	V
Reference Temperature Tolerance	V _{COLL} = 5.0V	19432*	1.291	1.3	1.309	V
		39432B	1.286	1.3	1.314	V
Reference Line Regulation	VCC = 2.4V to 36.0V, V _{COLL} = 5V	19432*		10	38	mV
		39432B		10	57	mV
Reference Load Regulation	I _{COLL} = 10mA to 50mA, V _{COLL} = 5V	19432*		10	38	mV
		39432B		10	57	mV
Reference Sink Current				10	μA	
Reference Source Current				–10	μA	
EA Input Bias Current			0.2	0.5	μA	
EA Input Offset Voltage		19432*		4.0	mV	
		39432B		4.0	mV	
EA Output Current Sink (Internally Limited)				16	μA	
EA Output Current Source				–1	mA	
Minimum Operating Current	VCC = 36.0V, V _{COLL} = 5V		0.50	0.80	mA	
Collector Current Limit (Note)	V _{COLL} = VCC = 36.0V, Ref = 1.35V ISET = GND		130	145	mA	
Collector Saturation	I _{COLL} = 20mA	0.7	1.1	1.5	V	
Transconductance (gm) (Note)	VCC = 2.4V to 36.0V, V _{COL} = 3V, I _{COLL} = 20mA ISET = GND	19432*	–170	–140	–110	mS
		39432B	–180	–140	–100	mS
Error Amplifier AVOL		60	90		dB	
Error Amplifier GBW	(Note 1)	3.0	5		MHz	
Transconductance Amplifier GBW			3		MHz	

* Also applies to the UC29432 and UC39432

Note: Programmed transconductance and collector current limit equations are specified in the ISET pin description.

Note1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

COLL: The collector of the output transistor with a maximum voltage of 36V. This pin is the output of the transconductance amplifier. The overall open loop voltage gain of the transconductance amplifier is $g_m \cdot R_L$, where g_m is designed to be $-140mS \pm 30mS$ and R_L represents the output load.

COMP: The output of the error amplifier and the input to the transconductance amplifier. This pin is available to compensate the high frequency gain of the error amplifier. It is internally voltage limited to approximately 2.0V.

EA+: The non-inverting input to the error amplifier.

GND: The reference and power ground for the device. The power ground of the output transistor is isolated on the chip from the substrate ground used to bias the remainder of the device.

ISET: The current set pin for the transconductance amplifier. The transconductance will be $-140mS$ as specified in the electrical table if this pin is grounded. If a resistance R_L is added to the ISET pin, the resulting new transconductance is calculated using the following equation: $g_m = -0.714V \cdot (5.1\Omega + R_L)$. The maximum current will be approximately

$$I_{MAX} = \frac{0.6V}{5.1\Omega + R_L}$$

REF: The output of the trimmed precision reference. It can source or sink $10\mu A$ and still maintain the 1% temperature specification.

SENSE: The inverting terminal of the error amplifier used as both the voltage sense input to the error amplifier and its other compensation point. The error amplifier uses the SENSE input to compare against the 1.3V on-chip reference.

The SENSE pin is also used as the undervoltage lockout (UVLO). It is intended to keep the chip from operating until the internal reference is properly biased. The threshold is approximately 1V. It is important that once the UVLO is released, the error amplifier can drive the transconductance amplifier to stabilize the loop. If a capacitor is connected between the SENSE and COMP pins to create a pole, it will limit the slew rate of the error amplifier. To increase the bandwidth and ensure startup at low load current, it is recommended to create a zero along with the pole as shown in the UC39431 shunt regulator application. The error amplifier must slew 2.0V to drive the transconductance amplifier initially on.

VCC: The power connection for the device. The minimum to maximum operating voltage is 2.2V to 36.0V. The quiescent current is typically 0.50mA.

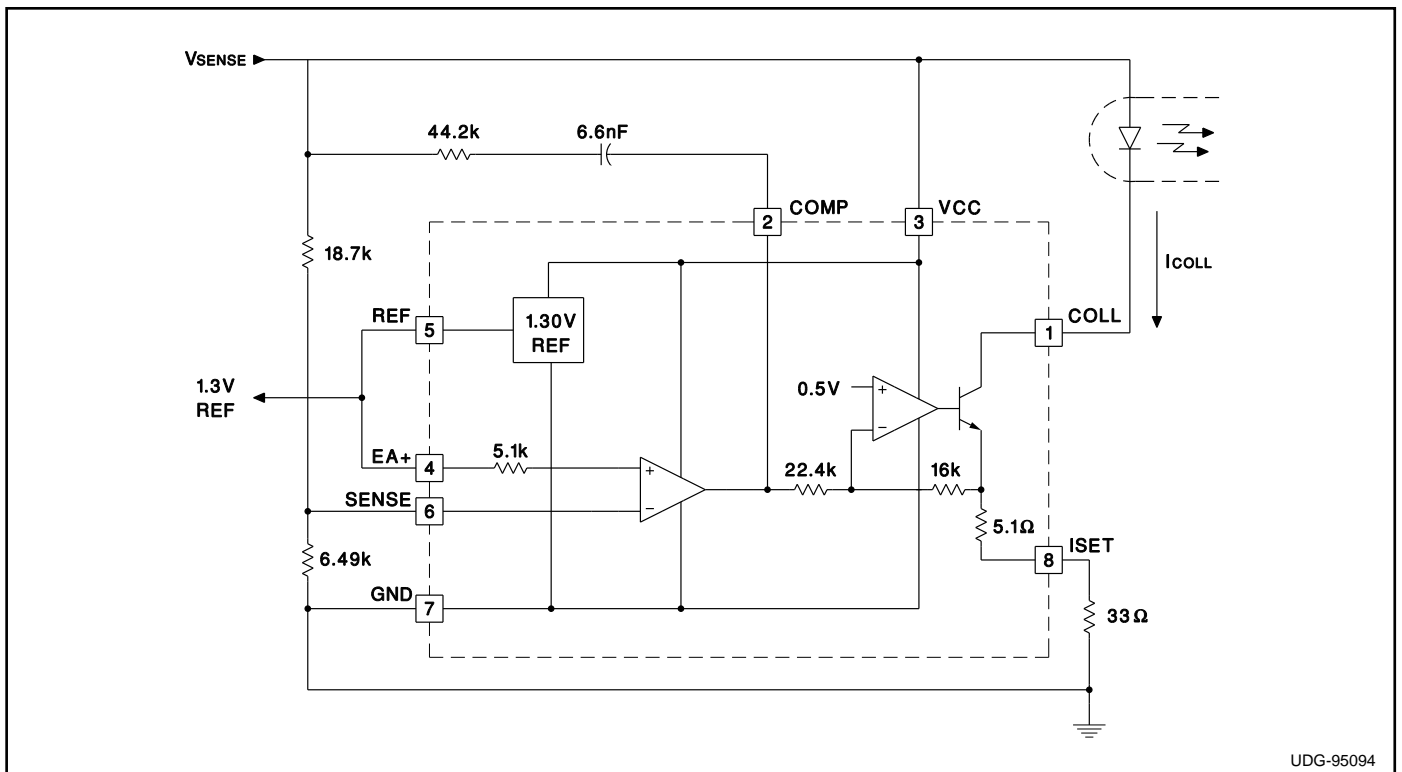


Figure 1. 5.0V Optocoupler Application

UDG-95094

OVERVOLTAGE COMPARATOR APPLICATION

The signal V_{IN} senses the input voltage. As long as the input voltage is less than 5.5V, the output is equal to the voltage on V_{IN} . During this region of operation, the diode is reversed biased which keeps the EA+ pin at 1.3V. When V_{IN} exceeds the over voltage threshold of 5.5V, the output is driven low. This forward biases the diode and creates hysteresis by changing the threshold to 4.5V.

OPTOCOUPLER APPLICATION

The optocoupler application shown takes advantage of the accessible pins REF and ISET. The ISET pin has a 33 ohm resistor to ground that protects the opto-coupler by limiting the current to about 16mA. This also lowers the transconductance to approximately 19mS. The ability to adjust the transconductance gives the designer further control of the loop gain. The REF pin is available to satisfy any high precision voltage requirements.

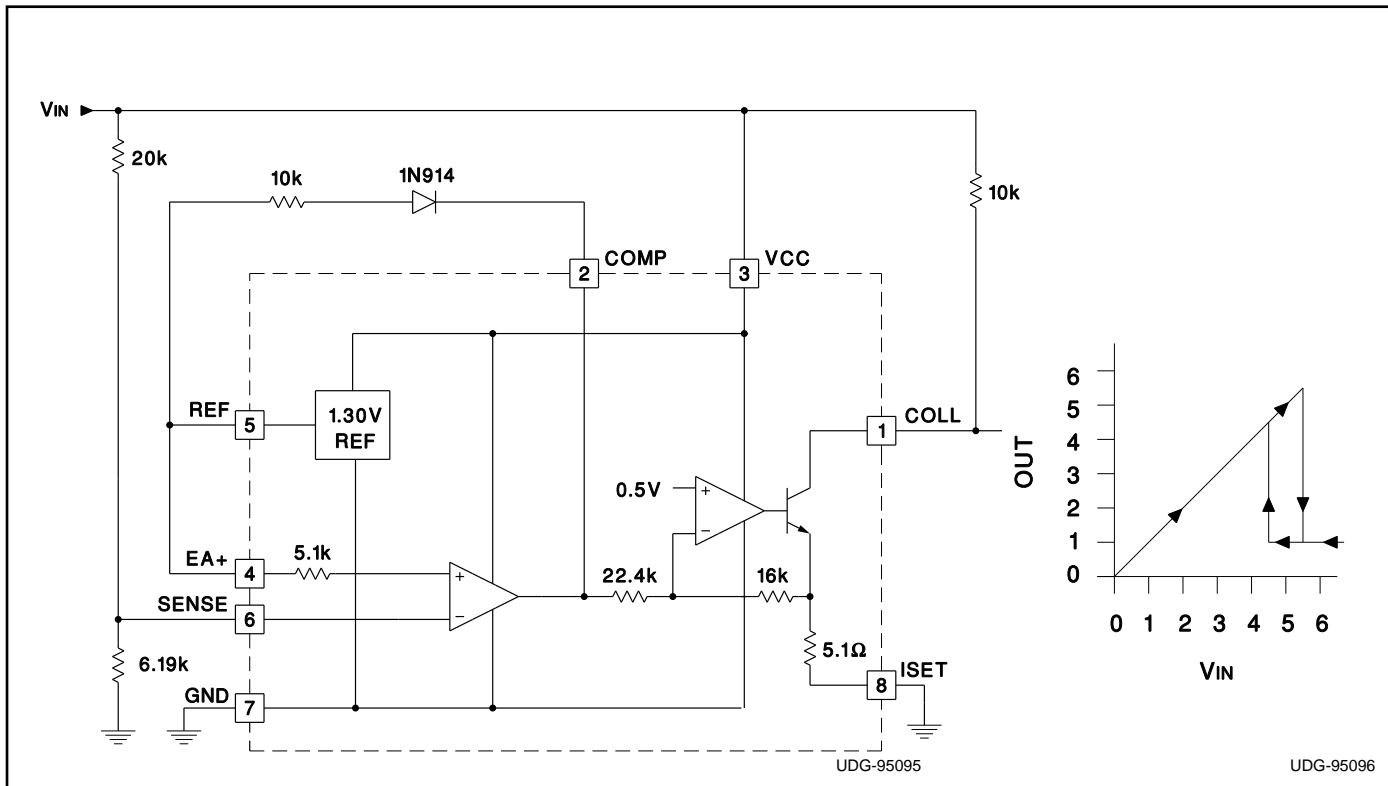


Figure 2. 5.5V Overvoltage Comparator With Hysteresis